REMARKS

This amendment responds to the final office action mailed July 30, 2003. In the office action the Examiner:

- rejected claims 1-9, 13, 14 and 16-22 under 35 U.S.C. 103(a) as being unpatentable over Cheney (U.S. Patent No. 5,668,599) in view of Orbits (U.S. Patent No. 5,630,097).

Claim Amendments

With this amendment, Applicants have amended claims 1 and 13 to recite that the buffer size assigned to the scalable buffer is dependent upon the first and second buffer sizes chosen by the buffer management module. Support for such amendment can be found in Fig. 5 and page 13, lines 3-9. Claims 9 and 22 have been amended for clarity. No new subject matter has been added. After entry of this amendment, the pending claims are: claims 1-9, 13, 14 and 16-22.

The rejections under 35 U.S.C. 103 should be withdrawn

The Examiner has rejected claims 1-9, 13, 14 and 16-22 under 35 U.S.C. 103(a) as being unpatentable over Cheney in view of Orbits. Applicants respectfully traverse the rejection.

To reject claims in an application under 35 U.S.C. § 103, the Examiner bears the initial burden of establishing a prima facie case of obviousness. *In re Bell*, 26 USPQ2d 1529, 1530 (Fed. Cir. 1993). In order to establish prima facie obviousness, the prior art, either alone or in combination, must teach or suggest each limitation of the rejected claims. See *In re Vaeck*, 20 USPQ2d 1438 (Fed. Cir. 1991); *In re Royka and Martin* 180 USPQ 580 (C.C.P.A. 1974); and *In re Wilson* 165 USPQ 494 (C.C.P.A. 1970). In the present instance, the cited arts fail to teach or suggest each limitation of the rejected claims.

Claim 13 is directed to a computer readable memory that directs a computer to function in a specified manner. The memory comprises a buffer management module to establish a buffer size for a scalable buffer and an analysis module to monitor the computer's cache memory performance when the scalable buffer is configured to the buffer size.

More specifically, the buffer management module establishes a first buffer size for the scalable buffer. In response, the analysis module analyzes the computer's cache memory performance and creates corresponding memory utilization data characterizing the cache memory performance. After that, the buffer management module establishes a second buffer

size for the scalable buffer, and the analysis module analyzes the computer's cache memory performance once again and creates corresponding memory utilization data. Through analyzing the memory utilization data in connection with the first and second buffer sizes, the analysis module selects an optimal buffer size to achieve low overall cache miss rate when the scalable buffer is configured to the optimal buffer size.

In other words, determining the optimal buffer size is a trial-and-error process. The variation of the overall cache miss rate is best characterized as a curve shown in Fig. 4c. To select an optimal buffer size, the analysis module needs to locate the bottom 430 on the curve by estimating the cache miss rate at multiple buffer sizes, including the first and second buffer sizes. Therefore, the optimal buffer size can be regarded as a function of the first and second buffer sizes through the memory utilization data (page 7, lines 19-32).

Cheney, however, relates to a system that minimizes the usage of a main memory, not a cache memory, through the use of a Spill Buffer in the main memory. While the Spill Buffer size may change, it varies only in accordance with parameters such as the operation modes and the frame sizes (Figs. 12-15) and there is no relationship or dependency between one and another Spill Buffer size. In other words, given a set of video decoding and displaying parameters, the Spill Buffer size is completely determined. Since Cheney does not teach a method of determining an optimal buffer size in accordance with first and second buffer sizes, the Spill Buffer in Cheney is not equivalent to the scalable buffer in Applicants' invention.

Even though Orbits discloses a cache management routine that is applied for reducing the cache miss rate, Orbits does not disclose a scalable buffer and a method of assigning a buffer size to the scalable buffer as recited in claim 13. Although there is a buffer 42 in Orbits for recording the sampled bus activity when a counter 41 overflows, Orbits does not suggest the size of the buffer 42 is scalable at all (Fig. 5 and column 6, lines 43-52).

Since Cheney and Orbits, either alone or in combination, do not teach or suggest the use of a scalable buffer and the method of determining its size as recited in claim 13, claim 13 and its dependent claims 14 and 16-22 are patentable over Cheney in view of Orbits.

Claim 1 is a method claim that has similar elements as claim 13. Therefore, claim 1 and its dependent claims 2-9 are also patentable over Cheney in view of Orbits.

In addition, claims 8 and 21 recite that the size of video data stream processing instructions is modified according to the buffer size selected by the analysis module, and

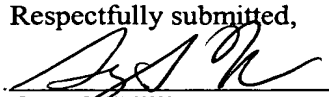
claims 9 and 22 further recite that the video data stream processing instructions are loop unrolled to match the buffer size selected by the analysis module.

Cheney, however, teaches the adjustment of a spill buffer to store picture **data** of different sizes, not video data stream processing **instructions**. The picture data of Cheney is different from video data stream processing instructions of claims 8, 9, 21, 22, as demonstrated by the fact that loop unrolling would not make sense with respect to picture data.

In light of the above amendments and remarks, Applicants respectfully request that the Examiner reconsider this application with a view towards allowance. The Examiner is invited to call the undersigned attorney at 650-849-7721, if a telephone call could help resolve any remaining items.

Respectfully submitted,

Date: September 30, 2003



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